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Docket No.: INF-P80224 US

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MAIL STOP: ~~APPEAL~~ BRIEF-PATENTS

By: ______________________ Date: February 4, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/734,467	Confirmation No. 5119
Inventor	:	Gerhard Beitel et al.	
Filed	:	December 11, 2000	
Title	:	Methods for Producing a Structured Metal Layer	
TC/A.U.	:	2822	
Examiner	:	J. L. Brophy	
Customer No.	**:**	**24131**	

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office Action dated August 7, 2003, finally rejecting claims 1-3, 7, 11-13, 15, 17 and 19-23.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

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Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-3, 7, 11-13, 15, 17 and 19-23 are rejected and are under appeal. Claims 8-10, 14, 16, 18 and 25-35 have been withdrawn from examination.

Appellants appreciatively acknowledge the Examiner's statement that claims 4-6 and 24 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

Status of Amendments:

No claims were amended after the final Office Action. *A Response under 37 CFR § 1.116* was filed on November 6, 2003. The Primary Examiner stated in an *Advisory Action* dated

December 3, 2003, that the request for reconsideration had been considered but did not place the application in condition for allowance.

In item 7 of the Advisory Action the Examiner stated that claims 4-6 and 24 were objected to (and allowable as indicated above) and also that claims 1-3, **5**, 7, 11-13, 17, and 19-23 were rejected. (emphasis added) Since claim 5 was indicated as being allowable and claim 15 was rejected in the Final Office Action, it is presumed that a typographical error was made in the Advisory Action and that the Examiner intended to reject claim 15 instead of claim 5. Accordingly, appellants will treat the rejection as including claim 15 rather than claim 5.

<u>Summary of the Invention</u>:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to methods for producing a structured metal layer, in particular a method for producing an electrode and, in particular, a method for producing an electrode for a storage capacitor of an integrated memory device.

Appellants explained on page 11 of the specification, line 14, that Fig. 1 shows a silicon substrate 1 with previously

fabricated transistors 4. Together with the storage capacitors still to be produced, the transistors form memory cells which serve the purpose of storing binary information. The transistors 4 each have two diffusion zones 2, which are disposed on the surface of the silicon substrate 1. The channel zones, which are separated from the gate electrodes 3 by the gate oxide on the surface of the silicon substrate 1, are disposed between the diffusion zones 2 of the transistors 4. The transistors 4 are produced using the methods known in the prior art, which are not explained here in more detail.

Appellants outlined on page 12 of the specification, line 1, that an insulating layer 5, for example an SiO_2 layer, is applied to the silicon substrate 1 bearing the transistors 4. Several insulating layers can also be applied, depending on the method used for producing the transistors 4. The structure resulting therefrom is shown in Fig. 1.

Appellants further outlined on page 12 of the specification, line 7, that the contact holes 6 are subsequently produced by a photographic technique. These contact holes 6 make a connection between the transistors 4 and the storage capacitors still to be produced. The contact holes 6 are produced, for example, by anisotropic etching with fluorine-containing gases. The resulting structure is shown in Fig. 2.

It is also stated on page 12 of the specification, line 14, that a conductive material 7, for example polysilicon doped in situ, is subsequently applied to the structure. This can be performed, for example, by a CVD method. The contact holes 6 are completely filled up by the application of the conductive material 7, and a continuous conductive layer is produced on the insulating layer 5 (Fig. 3). This is followed by a CMP step (Chemical Mechanical Polishing), which removes the continuous conductive layer on the surface of the insulating layer 5 and produces a flat surface.

As set forth in the last paragraph on page 12 of the specification, line 24, subsequently, depressions are formed in the insulating layer 5 in a fashion overlapping the contact holes 6. These depressions are now filled with barrier material 8, for example iridium oxide, up to a prescribed depth. This is performed by depositing the barrier material 8 over the entire surface and subsequently carrying out anisotropic etching. The anisotropic etching is carried out until the prescribed depth is achieved in the depressions. The structure produced thereby is shown in Fig. 4.

Appellants described on page 13 of the specification, line 8, that this concludes the first step a) of the method according to the invention. A prestructured substrate has been provided

to which the precious metal and/or the donor material can now subsequently be applied.

Appellants further described on page 13 of the specification, line 13, that, in this embodiment of the present invention, a precious metal, for example platinum is subsequently deposited over the entire surface of the structure shown in Fig. 4. The precious metal layer 9 is applied by a sputtering method at a temperature of approximately 500°C. The structure resulting therefrom is shown in Fig. 5. Subsequently, a titanium layer 10 is produced as donor material on the precious metal layer 9. This can be performed, for example, by a sputtering method. The structure resulting therefrom is shown in Fig. 6.

It is outlined in the last paragraph on page 13 of the specification, line 23, that heat treatment (annealing) then follows at a temperature of approximately 700°C such that the titanium of the titanium layer 10 diffuses as additive into the platinum layer 9, producing an alloy layer 11. The thickness of the titanium layer 10 is selected such that the titanium diffuses completely into the platinum layer 9 with the result that essentially no titanium remains behind on the surface of the alloy layer 11. The structure resulting therefrom is shown in Fig. 7.

Appellants explained on page 14 of the specification, line 7, that a CMP step is subsequently carried out, the alloy layer 11 being removed from the surface of the substrate. Only the portions of the alloy layer 11 located in the depressions above the barriers 8 remain behind. These parts of the alloy layer 11 later form the lower electrodes 12 for the still to be produced capacitors of the memory cells. A slurry with 1 to 5% by weight of abrasive Al_2O_3 particles and 2 to 10% by weight of H_2O_2 is used, for example, as oxidant for the CMP step. The use of a conventional slurry is possible, since the properties of the alloy layer are altered by the titanium which has diffused in such that chemical mechanical removal can be achieved even with conventional slurries.

It is further explained on page 14 of the specification, line 20, that after the CMP step, the insulating layer 5 is etched back by anisotropic etching so that the electrodes 12 protrude somewhat from the surface of the insulating layer 5. This appreciably increases the capacitor area of the storage capacitor still to be produced. A ferroelectric layer is then produced. An SBT film 13 is deposited with the aid of a CVD process onto the substrate thus prepared. The CVD process is carried out at a substrate temperature of 385°C and a chamber pressure of approximately 1200 Pa. The oxygen fraction in the gas mixture is 60%. In this way, the SBT film 13 is deposited

as an amorphous film. Consequently, the SBT film 13 essentially does not yet exhibit ferroelectric properties. The deposited, amorphous SBT 13 is subsequently annealed at a temperature of between 600 and 750°C for 10 to 30 minutes in an oxygen atmosphere, the ferroelectric properties of the SBT 13 being produced.

As set forth on page 15 of the specification, line 11, the upper electrode of the storage capacitors is subsequently deposited over the entire surface. Again, because of their good oxidation resistance and/or the formation of electrically conductive oxides, 4d and 5d transition metals, in particular platinum metals (Ru, Rh, Pd, Os, Ir, Pt) and especially platinum itself are used as electrode material. The precious metal layer 14, for example platinum, is applied, for example, by a sputtering method with a sputtering temperature of approximately 300 to 550°C. After the application of the upper electrode, annealing is carried out again in order to heal the boundary layer between the ferroelectric layer 13 and the upper electrode 14. The precious metal layer 14 and the ferroelectric layer 13 are subsequently structured with the aid of an anisotropic etching method so as to produce the structure shown in Fig. 8.

Appellants stated on page 16 of the specification, line 1, that the memory cells are thereby essentially completed. Further steps follow for the purpose of insulating the individual memory cells and of producing the wiring of the memory device. The methods used in this case belong, however, to the prior art and will not be explained here in more detail.

Appellants further stated on page 16 of the specification, line 7, that Figs. 9 to 12 show a further method for producing a structured layer according to a second exemplary embodiment of the invention. The first step a) of the method in accordance with the second embodiment of the present invention corresponds in this case to what was explained in connection with Figs. 1 to 4, and so repetition can be dispensed with.

It is outlined in the next to last paragraph on page 16 of the specification, line 14, that, also in this embodiment of the present invention, a precious metal, for example platinum, is deposited over the entire surface of the structure shown in Fig. 4. The precious metal layer 9 is applied by a sputtering method at a temperature of approximately 500°C. The structure resulting therefrom is shown in Fig. 9. A titanium oxide layer 15 is subsequently produced as donor material on the precious

metal layer 9. This can be performed, for example, by a CVD method. The structure resulting therefrom is shown in Fig. 10.

Appellants explained in the last paragraph on page 16 of the specification, line 24, that heat treatment (annealing) follows at a temperature of approximately 700°C in an oxygen atmosphere, such that the titanium of the titanium oxide layer 15 diffuses as additive into the platinum layer 9 and an alloy layer 16 is produced. A portion of the titanium also diffuses along the grain boundaries within the platinum layer 9. The titanium is oxidized by the oxygen of the oxygen atmosphere on the path along the grain boundaries, and so titanium oxide is also present along the grain boundaries. The heat treatment leaves a titanium oxide layer with a different stoichiometric composition on the alloy layer. This titanium oxide layer is removed from the alloy layer 16 by means of an additional etching step, for example with HF or HCL. The structure resulting therefrom is shown in Fig. 11.

Appellants described on page 17 of the specification, line 13, that a CMP step is subsequently carried out again, the alloy layer 16 being removed from the surface of the substrate. Only the parts of the alloy layer 16 which are disposed in the depressions above the barriers 8 remain behind. These parts of the alloy layer 16 later form the lower electrodes 12 for the

still to be produced capacitors of the memory cells. A slurry with 1 to 5% by weight of abrasive Al_2O_3 particles and 2 to 10% by weight of H_2O_2 is used, for example, as oxidant for the CMP step. The use of a conventional slurry is possible, since the properties of the alloy layer are altered by the titanium which has diffused in such that chemical mechanical removal can be achieved even with conventional slurries.

Appellants stated on page 18 of the specification, line 1, that this is followed again by etching back of the insulating layer 5, the application and annealing of the ferroelectric layer 13 and the application of the upper electrode 14 and the structuring of the upper electrode 14 and of the ferroelectric layer 13, resulting in the situation shown in Fig. 12.

Appellants further explained on page 18 of the specification, line 7, that Figs. 13 to 18 show a further method for producing a structured layer according to a third exemplary embodiment of the invention. The first steps of the method correspond in this case to what was explained in connection with Figs. 1 to 2, and so repetition can be dispensed with.

It is also outlined on page 18 of the specification, line 13, that conductive material 7, for example polysilicon doped in situ, is now applied to the structure. This can be performed,

for example, by a CVD method. The contact holes 6 are completely filled up by the application of the conductive material 7, and a continuous conductive layer is produced on the insulating layer 5 (Fig. 13). This is followed by a CMP step (Chemical Mechanical Polishing) which removes the continuous conductive layer on the surface of the insulating layer 5 and produces a flat surface.

As set forth in the last paragraph on page 18 of the specification, line 23, depressions in the insulating layer 5 are subsequently formed in a fashion overlapping the contact holes 6. These depressions are now filled down to a prescribed depth with barrier material 8, for example iridium oxide. This is performed by depositing the barrier material 8 over the entire surface (Fig. 14) and subsequently carrying out a CMP step. Subsequently, a further insulating layer 20, for example SiO_2, is deposited which is structured in accordance with the electrodes 12 still to be produced. The structure resulting therefrom is shown in Fig. 15.

Appellants stated on page 19 of the specification, line 8, that this concludes the first step a) of the method according to the invention. A prestructured substrate has been produced on which it is now possible subsequently to apply the precious metal and/or the donor material.

Appellants further stated on page 19 of the specification, line 13, that, in this embodiment of the present invention, a precious metal, for example platinum is subsequently deposited over the entire surface of the structure shown in Fig. 15. The precious metal layer 9 is applied by a sputtering method at a temperature of approximately 500°C. Subsequently, a titanium layer 10 is produced as donor material on the precious metal layer 9. This can be performed, for example, by a sputtering method. The structure resulting therefrom is shown in Fig. 16.

As set forth in the last paragraph on page 19 of the specification, line 22, heat treatment (annealing) then follows at a temperature of approximately 700°C such that the titanium of the titanium layer 10 diffuses as additive into the platinum layer 9, producing an alloy layer. The thickness of the titanium layer is selected such that the titanium diffuses completely into the platinum layer 9, with the result that essentially no titanium remains behind on the surface of the alloy layer.

Appellants outlined on page 20 of the specification, line 4, that a CMP step is subsequently carried out, the alloy layer being removed from the surface of the substrate. Only the portions of the alloy layer which are disposed in the depressions in the insulating layer 20 above the barriers 8

remain behind. These parts of the alloy layer later form the lower electrodes 12 for the still to be produced capacitors of the memory cells. A slurry with 1 to 5% by weight of abrasive Al_2O_3 particles and 2 to 10% by weight of H_2O_2 is used, for example, as oxidant for the CMP step. The use of a conventional slurry is possible, since the properties of the alloy layer are altered by the titanium which has diffused in such that chemical mechanical removal can be achieved even with conventional slurries.

Appellants outlined in the last paragraph on page 20 of the specification, line 18, that, after the CMP step, the insulating layer 20 is etched back by anisotropic etching so that the electrodes 12 protrudes somewhat from the surface of the insulating layer 20. This subsequently increases the capacitor area of the storage capacitor still to be produced. This is followed again by the application and annealing of the ferroelectric layer 13 and the application of the upper electrode 14 and the structuring of the upper electrode 14 and of the ferroelectric layer 13, resulting in the situation shown in Fig. 12.

<u>References Cited</u>:

U.S. Patent No. 5,708,302 (Azuma et al.), dated January 13, 1998;

U.S. Patent No. 5,952,687 (Kawakubo et al.), dated September 14, 1999;

U.S. Patent No. 5,976,928 (Kirlin et al.), dated November 2, 1999;

U.S. Patent No. 6,395,194 B1 (Russell et al.), dated May 28, 2002.

Issues

1. Whether or not claims 1-3, 7, 11-13, 15, and 17 are obvious over Kawakubo et al. (U.S. 5,952,687) (hereinafter "Kawakubo") in view of Azuma et al. (U.S. 5,708,302) (hereinafter "Azuma") under 35 U.S.C. § 103(a).

2. Whether or not claims 19-21 and 23 are obvious over Kawakubo in view of Azuma and further in view of Russell et al. (U.S. 6,395,194) (hereinafter "Russell") under 35 U.S.C. § 103(a).

3. Whether or not claims 19, 20, and 22 are obvious over Kawakubo in view of Azuma and further in view of Kirlin et al. (U.S. 5,976,928) (hereinafter "Kirlin") under 35 U.S.C. § 103(a).

Grouping of Claims:

Claim 1 is independent. Claims 2-3, 7, 11-13, 15, 17, and 19-23 depend on claim 1. The patentability of claims 19-23 is separately argued and the patentability of claims 2-3, 7, 11-13, 15, and 17 is not separately argued. Therefore, only claims 2-3, 7, 11-13, 15, and 17

stand or fall with claim 1.

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method of producing a structured layer, which has the following steps:

applying to the prestructured substrate a precious metal and a **donor material containing an additive which is not a precious metal** in two or more layers;

subjecting the layers to **heat treatment** at a temperature of between approximately 400°C and approximately 800°C, **such that the additive diffuses into the precious metal** and an alloy layer is produced; and

polishing the alloy layer by chemical and mechanical means. (emphasis added)

Regarding the second paragraph under "Claim Rejections - 35 USC § 103" on page 2 of the final Office Action of August 7, 2003, rejecting claims 1-3, 7, 11-13, 15, and 17 as being unpatentable over Kawakubo in view of Azuma under 35 U.S.C. § 103(a), it is noted that the Examiner stated that although Kawakubo does not disclose "that the bottom electrode is formed by applying a precious metal and a donor material and subjecting the layers to a heat treatment" it would have been obvious to one skilled in the art to modify Kawakubo using the method taught by Azuma " because a person skilled in the art...would have been motivated to use the method taught by Azuma et al in order to form a bottom electrode that adheres well to the underlying layers and does not have short-inducing irregularities...." It is submitted that this is an incorrect statement and is not sufficient motivation for the proposed combination of Azuma and Kawakubo, and is no more than an unsupported conclusionary statement based on hindsight and wishful thinking by the Examiner.

Kawakubo discloses (in Figs. 4A-4E) a method of manufacturing a memory cell with a switching transistor and a storage capacitor. Fig. 4B shows a prestructured substrate 1 with switching transistor 3, 4, 6a, 6b, a bit line 8, a contact plug 11, an insulating layer 9, and a polishing-stop layer 10.

A barrier metal film 12 made of titanium nitride is formed partly on the polishing stop layer 10 and partly on the inner surface of the trench (Fig. 4C). The bottom electrode 13 made of iridium is formed on the barrier metal film 12. Further, on the bottom electrode 13 a flattening insulating layer 16 made of boron silicate glass (BSG) is formed. The barrier film 12 can be made of titanium, tantalum, tantalum nitride or the like. Thereafter, as shown in Fig. 4D, those portions of the barrier metal film 12, bottom electrode 13 and insulating layer 16, which were deposited on or above the polishing stop layer 10, are removed by mechanical polishing. Mechanical polishing is used since the barrier metal film 12 and the bottom electrode 13 are very thin, 100 nm or less. See column 7, lines 48-66.

As stated by the Examiner, Kawabuko is deficient in that it does not disclose or teach "that the bottom electrode is formed by applying a precious metal and a donor material and subjecting the layers to a heat treatment." Nor does Kawabuko disclose an additive contained in the donor material, or even mention heat treatment as recited in the claims.

Azuma discloses a method for manufacturing a dielectric or ferroelectric integrated circuit capacitor with the emphasis on manufacturing a bottom electrode that adheres well and does

not have short-inducing surface irregularities due to the diffusion or blooming of silicon. Fig. 1 shows a capacitor 20 including substrate 22, bottom electrode 24, metal oxide layer 26, and top electrode 28. Bottom electrode 24 includes a plurality of respective layers including adhesion metal portion 34, first noble metal portion 36, diffusion barrier region 38, and second noble metal layer 40. Adhesion metal portion 34 is preferably made of Ti or Ta, first noble metal portion 36 is preferably made of Pt, but may also be Au, Ag, Pd, Ir, Rh, Ru, Os or conductive oxides of these metals. After deposition, portions 34 and 36 are preferably annealed to promote their interdiffusion, thereby providing barrier region 38. Region 38 is defined as the material between lower dashed line 42 and upper dashed line 44. Interface 50 is positioned between adhesion metal portion 34 and first noble metal portion 36, and represents the interlayer boundary at a time prior to the diffusion that forms barrier region 38 (see column 4, line 55 to column 5, line 20). The interdiffusion of portions 34 and 36 serves to increase the stability of the lattice, which correspondingly enhances resistance against diffusion through or from region 38 (see column 5, lines 38-41).

Appellants submit that claim 1 is not obvious over Kawakubo in view of Azuma.

The Examiner acknowledges that claim 1 differs from Kawakubo at least by the step of "subjecting the layers to a heat treatment." Appellants submit that this feature is novel and not obvious over Kawakubo in view of Azuma.

According to the present invention, layers made of precious metal are difficult to structure by a chemical-mechanical polishing (CMP) because of the chemical inertness of the material (see page 5, lines 9-25 of the instant specification).

The present invention solves this problem by introducing an additional donor material and heat treatment that allows for a "conventional CMP, in particular with the aid of conventional slurries, such as already used for structuring non-precious metals" (see page 7, lines 9-13 of the instant specification).

Kawakubo suggests the problem encountered during structuring precious metal bottom electrode layer 13 (see Figs. 14C-D) by disclosing that "[m]echanical polishing was used since the barrier metal film 12 and the bottom electrode 13 were very thin 100 nm or less …" and "…could be removed by chemical mechanical polishing which scarcely damages the objects being published" (see col. 7, line 64 to col. 8, line 3)

(underlining added). Thus, Kawakubo discloses that mechanical and/or chemical polishing of precious layers can be carried out only for very thin layers and with the risk of at least some damage to the objects being polished.

Therefore, a person skilled in the art who wants to structure a precious layer by a CMP step, starting out with the disclosure of Kawakubo, would logically look for methods that can polish precious layers without being limited to layers that have to be "very thin" or have "some damage" afterwards. Azuma does not address the problem disclosed by Kawakubo and, therefore, would not have even been considered for providing a solution to the problem disclosed by Kawakubo. Nor has the Examiner even shown any reason to modify Kawakubo in the first instance.

Accordingly, appellants respectfully submit that a person skilled in the art would not have been motivated to combine Kawakubo with Azuma to arrive at the claimed invention as suggested by the Examiner for the reasons discussed above. Therefore, the heating step of claim 1, namely, "subjecting the layers to heat treatment at a temperature of between approximately 400°C and approximately 800°C, such that the additive diffuses into the precious metal and an alloy layer is produced" is not obvious over Kawakubo in view of Azuma.

The Examiner also contends that "it would have been obvious...to modify the method disclosed by Kawakubo et al. by forming the bottom electrode using the method taught by Azuma et al because a person of ordinary skill...would have been motivated...to form a bottom electrode that adheres well to the underlying layers and does not have short-inducing surface irregularities."

Appellants submit that this statement is incorrect and without proper basis at least for the following reasons. Kawakubo does not disclose any problem relating to adherence of the bottom electrode to the underlying layers.

Moreover, Kawakubo already provides good adherence of the precious layer 13 to the underlying layers 11, 9 by barrier layer 12 between the two layers (see Fig. 4C-4D). Barrier layer 13 is made of "titanium, tantalum, tantalum nitride or the like" (column 7, lines 55-57), which are known to provide good adherence of precious metal layers to underlying layers (e.g., see Azuma column 1, lines 33-36).

Therefore, contrary to the Examiner's statement, a person skilled in the art would not have had sufficient motivation or reason to combine the disclosure of Azuma with Kawakubo as

proposed by the Examiner. Actually, one skilled in the art would refrain from any unnecessary heat treatments, since it is well-known in the semiconductor processing industry that it is important to minimize heating to reduce any possible damage to semiconductor devices. Thus, one skilled in the art would not go out of his or her way to do something that is contrary to good practice and inconsistent with established practices in the art to which the invention pertains.

Therefore, it is clearly apparent that a person skilled in the art would not combine Kawakubo with Azuma as proposed by the Examiner.

Azuma does not overcome the deficiencies of Kawakubo and for reasons discussed above a person skilled in the art would not combine Kawakubo and Azuma to obtain an improvement for a chemical mechanical polishing of a precious metal layer as recited in claim 1. The Examiner has not shown any teaching or basis in the primary reference of Kawakubo that would warrant or justify the proposed modification of Kawakubo by Azuma as proposed by the Examiner. The Examiner has merely stated that it would have been obvious to modify Kawakubo by Azuma "because a person of ordinary skill in the art...would have been motivated to use the method taught by Azuma...in

order to form a bottom electrode that adheres well to the underlying layers and does not have short-inducing irregularities...." However, while Azuma discloses that the substrate is heated in a diffusion furnace, the Examiner has not shown why Kawakubo would even want or need to be modified. One skilled in the art would not seek out a secondary reference unless there was a reason in the primary reference that justified or required modification. In this instance, it is submitted that the Examiner has not shown any reason to modify Kawabuko as proposed, and that the motivation suggested by the Examiner is in the secondary reference of Azuma and therefore, is insufficient reason to support modification of Kawabuko and the proposed combination of references.

Clearly, Kawakubo and Azuma do not show "applying to the prestructured substrate a precious metal and **a donor material containing an additive which is not a precious metal** in two or more layers; **subjecting the layers to heat treatment** at a temperature of between approximately 400°C and approximately 800°C, **such that the additive diffuses into the precious metal** and an **alloy layer is produced**; and **polishing the alloy layer by chemical and mechanical means"**, as recited in claim 1 of the instant application. (emphasis added)

Furthermore, in the Advisory Action dated December 3, 2003, the Examiner has stated that the request for reconsideration does not place the instant application in condition for allowance. Specifically, the Examiner incorrectly states that "applicant has failed to argue why the motivation provided in the rejection is not sufficient". On the contrary, appellants respectfully submit that they have argued why the combination of Azuma and Kawakubo is improper and moreover, why there is insufficient motivation to combine the references as proposed by the Examiner. Appellants have pointed out why one skilled in the art would not look to combine Kawakubo and Azuma and that for those reasons the basis for combining the references as suggested by the Examiner is deficient and insufficient and incorrect. That discussion is deemed more than sufficient to refute the Examiner's statements, which are based on conjecture and hindsight, and point out why the motivation stated by the Examiner is insufficient and deficient.

It is well settled that almost all claimed inventions are but novel combinations of old features. The courts have held in this context, however, that when "it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation **in the prior art** to make the selection made by the applicant". Interconnect Planning Corp. v. Feil, 227 USPQ

applicant". Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985) (emphasis added). "Obviousness can not be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination". In re Bond, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). "Under Section 103 teachings of references can be combined **only** if there is some suggestion or incentive to do so." ACS Hospital Systems, Inc. v. Montefiore Hospital et al., 221 USPQ 929, 933, 732 F.2d 1572 (Fed. Cir. 1984) (emphasis original). "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be '**clear and particular**.'" Winner Int'l Royalty Corp. v. Wang, 53 USPQ2d 1580, 1587, 202 F.3d 1340 (Fed. Cir. 2000) (emphasis added; citations omitted); Brown & Williamson Tobacco Corp. v. Philip Morris, Inc., 56 USPQ2d 1456, 1459 (Fed. Cir. Oct. 17, 2000). Appellants believe that there is no "clear and particular" teaching or suggestion in Kawakabu to incorporate the features of Azuma (as pointed out above by appellants), or for that matter the features of the other secondary references relied upon by the Examiner.

In establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of

ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in the art and not from the ***applicant's*** disclosure. See, for example, Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988), *cert. den.*, 488 U.S. 825 (1988). The Examiner has not provided the requisite or sufficient reason why one of ordinary skill in the art would have been led to modify Kawakubo or to combine Kawakubo's and Azuma's teachings to arrive at the claimed invention for providing a structured layer as claimed. Further, the Examiner has not shown the requisite motivation from some teaching, suggestion, or inference in Kawakubo to obtain the proposed combination of references.

Appellants respectfully believe that any teaching, suggestion, or incentive possibly derived from the prior art is only present with hindsight judgment in view of the claimed invention. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the appellant's structure as a template and selecting elements

from references to fill the gaps. The references **themselves** must provide some teaching whereby the applicant's combination would have been obvious." In re Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991) (emphasis added). In the instant rejection, no such teaching is present in or apparent from the cited prior art references.

Upon evaluation of the Examiner's response and statements, it is respectfully believed that the evidence adduced by the Examiner is insufficient to establish a prima facie case of obviousness with respect to the claims. Accordingly, the Honorable Board is therefore requested to reverse the final rejection of the Supervisory Primary Examiner.

Regarding the first full paragraph on page 4 under "Claim Rejections - 35 USC § 103" of the above-identified Office Action, rejecting claims 19-21 and 23 as being unpatentable over Kawakubo in view of Azuma and further in view of Russell et al. (U.S. 6,395,194) (hereinafter "Russell") under 35 U.S.C. § 103(a), the Examiner states that "it would have been obvious to a person of ordinary skill in the art...to modify...Kawakubo et al in view of Azuma et al by using a CMP slurry composition such as taught by Russell et al. because a person of ordinary skill in the art...would have been motivated to use the slurry taught by Russell et al in order

to selectively remove the noble metal layer during CMP...." It is respectfully submitted that this statement is incorrect and is no more than wishful thinking on the part of the Examiner based on hindsight reconstruction of the prior art to arrive at the claimed invention.

The foregoing discussion of Kawakubo and Azuma applies equally in the rejection of claims 19-21 and 23, which depend directly or indirectly on independent claim 1. Russell does not overcome the basic deficiencies of Kawakubo and Azuma, and certainly does not lend any credence to the proposed combination of these references. Therefore, the claims are believed patentable over the cited prior art for the reasons previously advanced.

Regarding the first full paragraph on page 5 under "Claim Rejections - 35 USC § 103" of the above-identified Office Action, rejecting claims 19, 20, and 22 as being unpatentable over Kawakubo in view of Azuma and further in view of Kirlin et al. (U.S. 5,976,928) (hereinafter "Kirlin") under 35 U.S.C. § 103(a), the Examiner states that the motivation for modifying Kawakubo and Azuma by Kirlin is "to use the slurry taught by Kirlin et al in order to effectively remove the metal and dielectric materials that are commonly used in capacitor structures...." It is respectfully submitted that

this statement is incorrect and is no more than wishful thinking on the part of the Examiner based on hindsight reconstruction of the prior art to arrive at the claimed invention.

The foregoing discussions of Kawakubo and Azuma are equally applicable in the instant rejection of claims 19, 20, and 22, which depend directly or indirectly on independent claim 1.

Kirlin does not make up for the deficiencies of Kawakubo and Azuma, individually or in the combination of these references. Therefore, claims 19, 20, and 22 are believed patentable over the prior art for the same reasons as previously advanced.

The Honorable Board is therefore respectfully urged to reverse the final rejection of the Supervisory Primary Examiner.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Appellants

FDP/bb

Date: February 4, 2004
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Appendix - Appealed Claims:

1. A method of producing a structured layer, which comprises the following steps:

providing a prestructured substrate;

applying to the prestructured substrate a precious metal and a donor material containing an additive which is not a precious metal in two or more layers;

subjecting the layers to heat treatment at a temperature of between approximately 400°C and approximately 800°C, such that the additive diffuses into the precious metal and an alloy layer is produced; and

polishing the alloy layer by chemical and mechanical means.

2. The method according to claim 1, wherein the donor material essentially comprises only the additive.

3. The method according to claim 1, which comprises applying the donor material to the substrate before the precious metal.

7. The method according to claim 1, wherein the thickness of the donor material is selected such that during heat treatment

the donor material essentially diffuses completely into the precious metal.

11. The method according to claim 1, wherein the precious metal is an element from Group 8b of the Periodic Table of the Elements and/or is Au.

12. The method according to claim 11, wherein the precious metal is from Group 8b of the Periodic Table of the Elements and/or is Ir.

13. The method according to claim 1, wherein the additive is Ti, TiO_x, Ta, W, Bi, Ru and/or Pd.

15. The method according to claim 1, wherein the donor material is Ti, TiO_x, TiN, Ta, TaN, W, WN, Bi, BiO_x, IrO_x, $IrHfO_x$, RuO_x and/or PdO_x.

17. The method according to claim 1, wherein the alloy layer produced contains between approximately 5 and approximately 30 atom % of the donor material.

19. The method according to claim 1, wherein a slurry containing water, abrasive particles and at least one oxidant is used for the chemical mechanical polishing.

20. The method according to claim 19, wherein Al_2O_3 particles or SiO_2 particles are used as the abrasive particles.

21. The method according to claim 19, wherein the abrasive particles have a size of approximately 50 to 300 nm.

22. The method according to claim 19, wherein H_2O_2 is used as the at least one oxidant.

23. The method according to claim 19, wherein the slurry has at least one stabilizer.

Docket No.: INF-P80224 US

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MAIL STOP: ~~APPEAL~~ BRIEF-PATENTS

By: ______________________ Date: February 4, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/734,467 Confirmation No. 5119
Inventor	:	Gerhard Beitel et al.
Filed	:	December 11, 2000
Title	:	Methods for Producing a Structured Metal Layer
TC/A.U.	:	2822
Examiner	:	J. L. Brophy
Customer No.	**:**	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir:

This is an appeal from the final rejection in the Office Action dated August 7, 2003, finally rejecting claims 1-3, 7, 11-13, 15, 17 and 19-23.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-3, 7, 11-13, 15, 17 and 19-23 are rejected and are under appeal. Claims 8-10, 14, 16, 18 and 25-35 have been withdrawn from examination.

Appellants appreciatively acknowledge the Examiner's statement that claims 4-6 and 24 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

Status of Amendments:

No claims were amended after the final Office Action. A *Response under 37 CFR § 1.116* was filed on November 6, 2003. The Primary Examiner stated in an *Advisory Action* dated

December 3, 2003, that the request for reconsideration had been considered but did not place the application in condition for allowance.

In item 7 of the Advisory Action the Examiner stated that claims 4-6 and 24 were objected to (and allowable as indicated above) and also that claims 1-3, **5**, 7, 11-13, 17, and 19-23 were rejected. (emphasis added) Since claim 5 was indicated as being allowable and claim 15 was rejected in the Final Office Action, it is presumed that a typographical error was made in the Advisory Action and that the Examiner intended to reject claim 15 instead of claim 5. Accordingly, appellants will treat the rejection as including claim 15 rather than claim 5.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to methods for producing a structured metal layer, in particular a method for producing an electrode and, in particular, a method for producing an electrode for a storage capacitor of an integrated memory device.

Appellants explained on page 11 of the specification, line 14, that Fig. 1 shows a silicon substrate 1 with previously

fabricated transistors 4. Together with the storage capacitors still to be produced, the transistors form memory cells which serve the purpose of storing binary information. The transistors 4 each have two diffusion zones 2, which are disposed on the surface of the silicon substrate 1. The channel zones, which are separated from the gate electrodes 3 by the gate oxide on the surface of the silicon substrate 1, are disposed between the diffusion zones 2 of the transistors 4. The transistors 4 are produced using the methods known in the prior art, which are not explained here in more detail.

Appellants outlined on page 12 of the specification, line 1, that an insulating layer 5, for example an SiO_2 layer, is applied to the silicon substrate 1 bearing the transistors 4. Several insulating layers can also be applied, depending on the method used for producing the transistors 4. The structure resulting therefrom is shown in Fig. 1.

Appellants further outlined on page 12 of the specification, line 7, that the contact holes 6 are subsequently produced by a photographic technique. These contact holes 6 make a connection between the transistors 4 and the storage capacitors still to be produced. The contact holes 6 are produced, for example, by anisotropic etching with fluorine-containing gases. The resulting structure is shown in Fig. 2.

It is also stated on page 12 of the specification, line 14, that a conductive material 7, for example polysilicon doped in situ, is subsequently applied to the structure. This can be performed, for example, by a CVD method. The contact holes 6 are completely filled up by the application of the conductive material 7, and a continuous conductive layer is produced on the insulating layer 5 (Fig. 3). This is followed by a CMP step (Chemical Mechanical Polishing), which removes the continuous conductive layer on the surface of the insulating layer 5 and produces a flat surface.

As set forth in the last paragraph on page 12 of the specification, line 24, subsequently, depressions are formed in the insulating layer 5 in a fashion overlapping the contact holes 6. These depressions are now filled with barrier material 8, for example iridium oxide, up to a prescribed depth. This is performed by depositing the barrier material 8 over the entire surface and subsequently carrying out anisotropic etching. The anisotropic etching is carried out until the prescribed depth is achieved in the depressions. The structure produced thereby is shown in Fig. 4.

Appellants described on page 13 of the specification, line 8, that this concludes the first step a) of the method according to the invention. A prestructured substrate has been provided

to which the precious metal and/or the donor material can now subsequently be applied.

Appellants further described on page 13 of the specification, line 13, that, in this embodiment of the present invention, a precious metal, for example platinum is subsequently deposited over the entire surface of the structure shown in Fig. 4. The precious metal layer 9 is applied by a sputtering method at a temperature of approximately 500°C. The structure resulting therefrom is shown in Fig. 5. Subsequently, a titanium layer 10 is produced as donor material on the precious metal layer 9. This can be performed, for example, by a sputtering method. The structure resulting therefrom is shown in Fig. 6.

It is outlined in the last paragraph on page 13 of the specification, line 23, that heat treatment (annealing) then follows at a temperature of approximately 700°C such that the titanium of the titanium layer 10 diffuses as additive into the platinum layer 9, producing an alloy layer 11. The thickness of the titanium layer 10 is selected such that the titanium diffuses completely into the platinum layer 9 with the result that essentially no titanium remains behind on the surface of the alloy layer 11. The structure resulting therefrom is shown in Fig. 7.

Appellants explained on page 14 of the specification, line 7, that a CMP step is subsequently carried out, the alloy layer 11 being removed from the surface of the substrate. Only the portions of the alloy layer 11 located in the depressions above the barriers 8 remain behind. These parts of the alloy layer 11 later form the lower electrodes 12 for the still to be produced capacitors of the memory cells. A slurry with 1 to 5% by weight of abrasive Al_2O_3 particles and 2 to 10% by weight of H_2O_2 is used, for example, as oxidant for the CMP step. The use of a conventional slurry is possible, since the properties of the alloy layer are altered by the titanium which has diffused in such that chemical mechanical removal can be achieved even with conventional slurries.

It is further explained on page 14 of the specification, line 20, that after the CMP step, the insulating layer 5 is etched back by anisotropic etching so that the electrodes 12 protrude somewhat from the surface of the insulating layer 5. This appreciably increases the capacitor area of the storage capacitor still to be produced. A ferroelectric layer is then produced. An SBT film 13 is deposited with the aid of a CVD process onto the substrate thus prepared. The CVD process is carried out at a substrate temperature of 385°C and a chamber pressure of approximately 1200 Pa. The oxygen fraction in the gas mixture is 60%. In this way, the SBT film 13 is deposited

as an amorphous film. Consequently, the SBT film 13 essentially does not yet exhibit ferroelectric properties. The deposited, amorphous SBT 13 is subsequently annealed at a temperature of between 600 and 750°C for 10 to 30 minutes in an oxygen atmosphere, the ferroelectric properties of the SBT 13 being produced.

As set forth on page 15 of the specification, line 11, the upper electrode of the storage capacitors is subsequently deposited over the entire surface. Again, because of their good oxidation resistance and/or the formation of electrically conductive oxides, 4d and 5d transition metals, in particular platinum metals (Ru, Rh, Pd, Os, Ir, Pt) and especially platinum itself are used as electrode material. The precious metal layer 14, for example platinum, is applied, for example, by a sputtering method with a sputtering temperature of approximately 300 to 550°C. After the application of the upper electrode, annealing is carried out again in order to heal the boundary layer between the ferroelectric layer 13 and the upper electrode 14. The precious metal layer 14 and the ferroelectric layer 13 are subsequently structured with the aid of an anisotropic etching method so as to produce the structure shown in Fig. 8.

Appellants stated on page 16 of the specification, line 1, that the memory cells are thereby essentially completed. Further steps follow for the purpose of insulating the individual memory cells and of producing the wiring of the memory device. The methods used in this case belong, however, to the prior art and will not be explained here in more detail.

Appellants further stated on page 16 of the specification, line 7, that Figs. 9 to 12 show a further method for producing a structured layer according to a second exemplary embodiment of the invention. The first step a) of the method in accordance with the second embodiment of the present invention corresponds in this case to what was explained in connection with Figs. 1 to 4, and so repetition can be dispensed with.

It is outlined in the next to last paragraph on page 16 of the specification, line 14, that, also in this embodiment of the present invention, a precious metal, for example platinum, is deposited over the entire surface of the structure shown in Fig. 4. The precious metal layer 9 is applied by a sputtering method at a temperature of approximately 500°C. The structure resulting therefrom is shown in Fig. 9. A titanium oxide layer 15 is subsequently produced as donor material on the precious

metal layer 9. This can be performed, for example, by a CVD method. The structure resulting therefrom is shown in Fig. 10.

Appellants explained in the last paragraph on page 16 of the specification, line 24, that heat treatment (annealing) follows at a temperature of approximately 700°C in an oxygen atmosphere, such that the titanium of the titanium oxide layer 15 diffuses as additive into the platinum layer 9 and an alloy layer 16 is produced. A portion of the titanium also diffuses along the grain boundaries within the platinum layer 9. The titanium is oxidized by the oxygen of the oxygen atmosphere on the path along the grain boundaries, and so titanium oxide is also present along the grain boundaries. The heat treatment leaves a titanium oxide layer with a different stoichiometric composition on the alloy layer. This titanium oxide layer is removed from the alloy layer 16 by means of an additional etching step, for example with HF or HCL. The structure resulting therefrom is shown in Fig. 11.

Appellants described on page 17 of the specification, line 13, that a CMP step is subsequently carried out again, the alloy layer 16 being removed from the surface of the substrate. Only the parts of the alloy layer 16 which are disposed in the depressions above the barriers 8 remain behind. These parts of the alloy layer 16 later form the lower electrodes 12 for the

still to be produced capacitors of the memory cells. A slurry with 1 to 5% by weight of abrasive Al_2O_3 particles and 2 to 10% by weight of H_2O_2 is used, for example, as oxidant for the CMP step. The use of a conventional slurry is possible, since the properties of the alloy layer are altered by the titanium which has diffused in such that chemical mechanical removal can be achieved even with conventional slurries.

Appellants stated on page 18 of the specification, line 1, that this is followed again by etching back of the insulating layer 5, the application and annealing of the ferroelectric layer 13 and the application of the upper electrode 14 and the structuring of the upper electrode 14 and of the ferroelectric layer 13, resulting in the situation shown in Fig. 12.

Appellants further explained on page 18 of the specification, line 7, that Figs. 13 to 18 show a further method for producing a structured layer according to a third exemplary embodiment of the invention. The first steps of the method correspond in this case to what was explained in connection with Figs. 1 to 2, and so repetition can be dispensed with.

It is also outlined on page 18 of the specification, line 13, that conductive material 7, for example polysilicon doped in situ, is now applied to the structure. This can be performed,

for example, by a CVD method. The contact holes 6 are completely filled up by the application of the conductive material 7, and a continuous conductive layer is produced on the insulating layer 5 (Fig. 13). This is followed by a CMP step (Chemical Mechanical Polishing) which removes the continuous conductive layer on the surface of the insulating layer 5 and produces a flat surface.

As set forth in the last paragraph on page 18 of the specification, line 23, depressions in the insulating layer 5 are subsequently formed in a fashion overlapping the contact holes 6. These depressions are now filled down to a prescribed depth with barrier material 8, for example iridium oxide. This is performed by depositing the barrier material 8 over the entire surface (Fig. 14) and subsequently carrying out a CMP step. Subsequently, a further insulating layer 20, for example SiO_2, is deposited which is structured in accordance with the electrodes 12 still to be produced. The structure resulting therefrom is shown in Fig. 15.

Appellants stated on page 19 of the specification, line 8, that this concludes the first step a) of the method according to the invention. A prestructured substrate has been produced on which it is now possible subsequently to apply the precious metal and/or the donor material.

Appellants further stated on page 19 of the specification, line 13, that, in this embodiment of the present invention, a precious metal, for example platinum is subsequently deposited over the entire surface of the structure shown in Fig. 15. The precious metal layer 9 is applied by a sputtering method at a temperature of approximately 500°C. Subsequently, a titanium layer 10 is produced as donor material on the precious metal layer 9. This can be performed, for example, by a sputtering method. The structure resulting therefrom is shown in Fig. 16.

As set forth in the last paragraph on page 19 of the specification, line 22, heat treatment (annealing) then follows at a temperature of approximately 700°C such that the titanium of the titanium layer 10 diffuses as additive into the platinum layer 9, producing an alloy layer. The thickness of the titanium layer is selected such that the titanium diffuses completely into the platinum layer 9, with the result that essentially no titanium remains behind on the surface of the alloy layer.

Appellants outlined on page 20 of the specification, line 4, that a CMP step is subsequently carried out, the alloy layer being removed from the surface of the substrate. Only the portions of the alloy layer which are disposed in the depressions in the insulating layer 20 above the barriers 8

remain behind. These parts of the alloy layer later form the lower electrodes 12 for the still to be produced capacitors of the memory cells. A slurry with 1 to 5% by weight of abrasive Al_2O_3 particles and 2 to 10% by weight of H_2O_2 is used, for example, as oxidant for the CMP step. The use of a conventional slurry is possible, since the properties of the alloy layer are altered by the titanium which has diffused in such that chemical mechanical removal can be achieved even with conventional slurries.

Appellants outlined in the last paragraph on page 20 of the specification, line 18, that, after the CMP step, the insulating layer 20 is etched back by anisotropic etching so that the electrodes 12 protrudes somewhat from the surface of the insulating layer 20. This subsequently increases the capacitor area of the storage capacitor still to be produced. This is followed again by the application and annealing of the ferroelectric layer 13 and the application of the upper electrode 14 and the structuring of the upper electrode 14 and of the ferroelectric layer 13, resulting in the situation shown in Fig. 12.

<u>References Cited</u>:

U.S. Patent No. 5,708,302 (Azuma et al.), dated January 13, 1998;

U.S. Patent No. 5,952,687 (Kawakubo et al.), dated September 14, 1999;

U.S. Patent No. 5,976,928 (Kirlin et al.), dated November 2, 1999;

U.S. Patent No. 6,395,194 B1 (Russell et al.), dated May 28, 2002.

Issues

1. Whether or not claims 1-3, 7, 11-13, 15, and 17 are obvious over Kawakubo et al. (U.S. 5,952,687) (hereinafter "Kawakubo") in view of Azuma et al. (U.S. 5,708,302) (hereinafter "Azuma") under 35 U.S.C. § 103(a).

2. Whether or not claims 19-21 and 23 are obvious over Kawakubo in view of Azuma and further in view of Russell et al. (U.S. 6,395,194) (hereinafter "Russell") under 35 U.S.C. § 103(a).

3. Whether or not claims 19, 20, and 22 are obvious over Kawakubo in view of Azuma and further in view of Kirlin et al. (U.S. 5,976,928) (hereinafter "Kirlin") under 35 U.S.C. § 103(a).

Grouping of Claims:

Claim 1 is independent. Claims 2-3, 7, 11-13, 15, 17, and 19-23 depend on claim 1. The patentability of claims 19-23 is separately argued and the patentability of claims 2-3, 7, 11-13, 15, and 17 is not separately argued. Therefore, only claims 2-3, 7, 11-13, 15, and 17 stand or fall with claim 1.

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method of producing a structured layer, which has the following steps:

applying to the prestructured substrate a precious metal and a **donor material containing an additive which is not a precious metal** in two or more layers;

subjecting the layers to **heat treatment** at a temperature of between approximately 400°C and approximately 800°C, **such that the additive diffuses into the precious metal** and an alloy layer is produced; and

polishing the alloy layer by chemical and mechanical means. (emphasis added)

Regarding the second paragraph under "Claim Rejections - 35 USC § 103" on page 2 of the final Office Action of August 7, 2003, rejecting claims 1-3, 7, 11-13, 15, and 17 as being unpatentable over Kawakubo in view of Azuma under 35 U.S.C. § 103(a), it is noted that the Examiner stated that although Kawakubo does not disclose "that the bottom electrode is formed by applying a precious metal and a donor material and subjecting the layers to a heat treatment" it would have been obvious to one skilled in the art to modify Kawakubo using the method taught by Azuma " because a person skilled in the art...would have been motivated to use the method taught by Azuma et al in order to form a bottom electrode that adheres well to the underlying layers and does not have short-inducing irregularities...." It is submitted that this is an incorrect statement and is not sufficient motivation for the proposed combination of Azuma and Kawakubo, and is no more than an unsupported conclusionary statement based on hindsight and wishful thinking by the Examiner.

Kawakubo discloses (in Figs. 4A-4E) a method of manufacturing a memory cell with a switching transistor and a storage capacitor. Fig. 4B shows a prestructured substrate 1 with switching transistor 3, 4, 6a, 6b, a bit line 8, a contact plug 11, an insulating layer 9, and a polishing-stop layer 10.

A barrier metal film 12 made of titanium nitride is formed partly on the polishing stop layer 10 and partly on the inner surface of the trench (Fig. 4C). The bottom electrode 13 made of iridium is formed on the barrier metal film 12. Further, on the bottom electrode 13 a flattening insulating layer 16 made of boron silicate glass (BSG) is formed. The barrier film 12 can be made of titanium, tantalum, tantalum nitride or the like. Thereafter, as shown in Fig. 4D, those portions of the barrier metal film 12, bottom electrode 13 and insulating layer 16, which were deposited on or above the polishing stop layer 10, are removed by mechanical polishing. Mechanical polishing is used since the barrier metal film 12 and the bottom electrode 13 are very thin, 100 nm or less. See column 7, lines 48-66.

As stated by the Examiner, Kawabuko is deficient in that it does not disclose or teach "that the bottom electrode is formed by applying a precious metal and a donor material and subjecting the layers to a heat treatment." Nor does Kawabuko disclose an additive contained in the donor material, or even mention heat treatment as recited in the claims.

Azuma discloses a method for manufacturing a dielectric or ferroelectric integrated circuit capacitor with the emphasis on manufacturing a bottom electrode that adheres well and does

not have short-inducing surface irregularities due to the diffusion or blooming of silicon. Fig. 1 shows a capacitor 20 including substrate 22, bottom electrode 24, metal oxide layer 26, and top electrode 28. Bottom electrode 24 includes a plurality of respective layers including adhesion metal portion 34, first noble metal portion 36, diffusion barrier region 38, and second noble metal layer 40. Adhesion metal portion 34 is preferably made of Ti or Ta, first noble metal portion 36 is preferably made of Pt, but may also be Au, Ag, Pd, Ir, Rh, Ru, Os or conductive oxides of these metals. After deposition, portions 34 and 36 are preferably annealed to promote their interdiffusion, thereby providing barrier region 38. Region 38 is defined as the material between lower dashed line 42 and upper dashed line 44. Interface 50 is positioned between adhesion metal portion 34 and first noble metal portion 36, and represents the interlayer boundary at a time prior to the diffusion that forms barrier region 38 (see column 4, line 55 to column 5, line 20). The interdiffusion of portions 34 and 36 serves to increase the stability of the lattice, which correspondingly enhances resistance against diffusion through or from region 38 (see column 5, lines 38-41).

Appellants submit that claim 1 is not obvious over Kawakubo in view of Azuma.

The Examiner acknowledges that claim 1 differs from Kawakubo at least by the step of "subjecting the layers to a heat treatment." Appellants submit that this feature is novel and not obvious over Kawakubo in view of Azuma.

According to the present invention, layers made of precious metal are difficult to structure by a chemical-mechanical polishing (CMP) because of the chemical inertness of the material (see page 5, lines 9-25 of the instant specification).

The present invention solves this problem by introducing an additional donor material and heat treatment that allows for a "conventional CMP, in particular with the aid of conventional slurries, such as already used for structuring non-precious metals" (see page 7, lines 9-13 of the instant specification).

Kawakubo suggests the problem encountered during structuring precious metal bottom electrode layer 13 (see Figs. 14C-D) by disclosing that "[m]echanical polishing was used since the barrier metal film 12 and the bottom electrode 13 were very thin 100 nm or less …" and "…could be removed by chemical mechanical polishing which scarcely damages the objects being published" (see col. 7, line 64 to col. 8, line 3)

(underlining added). Thus, Kawakubo discloses that mechanical and/or chemical polishing of precious layers can be carried out only for very thin layers and with the risk of at least some damage to the objects being polished.

Therefore, a person skilled in the art who wants to structure a precious layer by a CMP step, starting out with the disclosure of Kawakubo, would logically look for methods that can polish precious layers without being limited to layers that have to be "very thin" or have "some damage" afterwards. Azuma does not address the problem disclosed by Kawakubo and, therefore, would not have even been considered for providing a solution to the problem disclosed by Kawakubo. Nor has the Examiner even shown any reason to modify Kawakubo in the first instance.

Accordingly, appellants respectfully submit that a person skilled in the art would not have been motivated to combine Kawakubo with Azuma to arrive at the claimed invention as suggested by the Examiner for the reasons discussed above. Therefore, the heating step of claim 1, namely, "subjecting the layers to heat treatment at a temperature of between approximately 400°C and approximately 800°C, such that the additive diffuses into the precious metal and an alloy layer is produced" is not obvious over Kawakubo in view of Azuma.

The Examiner also contends that "it would have been obvious...to modify the method disclosed by Kawakubo et al. by forming the bottom electrode using the method taught by Azuma et al because a person of ordinary skill...would have been motivated...to form a bottom electrode that adheres well to the underlying layers and does not have short-inducing surface irregularities."

Appellants submit that this statement is incorrect and without proper basis at least for the following reasons. Kawakubo does not disclose any problem relating to adherence of the bottom electrode to the underlying layers.

Moreover, Kawakubo already provides good adherence of the precious layer 13 to the underlying layers 11, 9 by barrier layer 12 between the two layers (see Fig. 4C-4D). Barrier layer 13 is made of "titanium, tantalum, tantalum nitride or the like" (column 7, lines 55-57), which are known to provide good adherence of precious metal layers to underlying layers (e.g., see Azuma column 1, lines 33-36).

Therefore, contrary to the Examiner's statement, a person skilled in the art would not have had sufficient motivation or reason to combine the disclosure of Azuma with Kawakubo as

proposed by the Examiner. Actually, one skilled in the art would refrain from any unnecessary heat treatments, since it is well-known in the semiconductor processing industry that it is important to minimize heating to reduce any possible damage to semiconductor devices. Thus, one skilled in the art would not go out of his or her way to do something that is contrary to good practice and inconsistent with established practices in the art to which the invention pertains.

Therefore, it is clearly apparent that a person skilled in the art would not combine Kawakubo with Azuma as proposed by the Examiner.

Azuma does not overcome the deficiencies of Kawakubo and for reasons discussed above a person skilled in the art would not combine Kawakubo and Azuma to obtain an improvement for a chemical mechanical polishing of a precious metal layer as recited in claim 1. The Examiner has not shown any teaching or basis in the primary reference of Kawakubo that would warrant or justify the proposed modification of Kawakubo by Azuma as proposed by the Examiner. The Examiner has merely stated that it would have been obvious to modify Kawakubo by Azuma "because a person of ordinary skill in the art...would have been motivated to use the method taught by Azuma...in

order to form a bottom electrode that adheres well to the underlying layers and does not have short-inducing irregularities...." However, while Azuma discloses that the substrate is heated in a diffusion furnace, the Examiner has not shown why Kawakubo would even want or need to be modified. One skilled in the art would not seek out a secondary reference unless there was a reason in the primary reference that justified or required modification. In this instance, it is submitted that the Examiner has not shown any reason to modify Kawabuko as proposed, and that the motivation suggested by the Examiner is in the secondary reference of Azuma and therefore, is insufficient reason to support modification of Kawabuko and the proposed combination of references.

Clearly, Kawakubo and Azuma do not show "applying to the prestructured substrate a precious metal and **a donor material containing an additive which is not a precious metal** in two or more layers; **subjecting the layers to heat treatment** at a temperature of between approximately 400°C and approximately 800°C, **such that the additive diffuses into the precious metal** and an **alloy layer is produced**; and **polishing the alloy layer by chemical and mechanical means"**, as recited in claim 1 of the instant application. (emphasis added)

Furthermore, in the Advisory Action dated December 3, 2003, the Examiner has stated that the request for reconsideration does not place the instant application in condition for allowance. Specifically, the Examiner incorrectly states that "applicant has failed to argue why the motivation provided in the rejection is not sufficient". On the contrary, appellants respectfully submit that they have argued why the combination of Azuma and Kawakubo is improper and moreover, why there is insufficient motivation to combine the references as proposed by the Examiner. Appellants have pointed out why one skilled in the art would not look to combine Kawakubo and Azuma and that for those reasons the basis for combining the references as suggested by the Examiner is deficient and insufficient and incorrect. That discussion is deemed more than sufficient to refute the Examiner's statements, which are based on conjecture and hindsight, and point out why the motivation stated by the Examiner is insufficient and deficient.

It is well settled that almost all claimed inventions are but novel combinations of old features. The courts have held in this context, however, that when "it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation **in the prior art** to make the selection made by the applicant". Interconnect Planning Corp. v. Feil, 227 USPQ

applicant". Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985) (emphasis added). "Obviousness can not be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination". In re Bond, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). "Under Section 103 teachings of references can be combined **only** if there is some suggestion or incentive to do so." ACS Hospital Systems, Inc. v. Montefiore Hospital et al., 221 USPQ 929, 933, 732 F.2d 1572 (Fed. Cir. 1984) (emphasis original). "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be '**clear and particular.**'" Winner Int'l Royalty Corp. v. Wang, 53 USPQ2d 1580, 1587, 202 F.3d 1340 (Fed. Cir. 2000) (emphasis added; citations omitted); Brown & Williamson Tobacco Corp. v. Philip Morris, Inc., 56 USPQ2d 1456, 1459 (Fed. Cir. Oct. 17, 2000). Appellants believe that there is no "clear and particular" teaching or suggestion in Kawakabu to incorporate the features of Azuma (as pointed out above by appellants), or for that matter the features of the other secondary references relied upon by the Examiner.

In establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of

ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in the art and not from the ***applicant's*** disclosure. See, for example, Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988), *cert. den.*, 488 U.S. 825 (1988). The Examiner has not provided the requisite or sufficient reason why one of ordinary skill in the art would have been led to modify Kawakubo or to combine Kawakubo's and Azuma's teachings to arrive at the claimed invention for providing a structured layer as claimed. Further, the Examiner has not shown the requisite motivation from some teaching, suggestion, or inference in Kawakubo to obtain the proposed combination of references.

Appellants respectfully believe that any teaching, suggestion, or incentive possibly derived from the prior art is only present with hindsight judgment in view of the claimed invention. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the appellant's structure as a template and selecting elements

from references to fill the gaps. The references **themselves** must provide some teaching whereby the applicant's combination would have been obvious." In re Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991) (emphasis added). In the instant rejection, no such teaching is present in or apparent from the cited prior art references.

Upon evaluation of the Examiner's response and statements, it is respectfully believed that the evidence adduced by the Examiner is insufficient to establish a prima facie case of obviousness with respect to the claims. Accordingly, the Honorable Board is therefore requested to reverse the final rejection of the Supervisory Primary Examiner.

Regarding the first full paragraph on page 4 under "Claim Rejections - 35 USC § 103" of the above-identified Office Action, rejecting claims 19-21 and 23 as being unpatentable over Kawakubo in view of Azuma and further in view of Russell et al. (U.S. 6,395,194) (hereinafter "Russell") under 35 U.S.C. § 103(a), the Examiner states that "it would have been obvious to a person of ordinary skill in the art...to modify...Kawakubo et al in view of Azuma et al by using a CMP slurry composition such as taught by Russell et al. because a person of ordinary skill in the art...would have been motivated to use the slurry taught by Russell et al in order

to selectively remove the noble metal layer during CMP...." It is respectfully submitted that this statement is incorrect and is no more than wishful thinking on the part of the Examiner based on hindsight reconstruction of the prior art to arrive at the claimed invention.

The foregoing discussion of Kawakubo and Azuma applies equally in the rejection of claims 19-21 and 23, which depend directly or indirectly on independent claim 1. Russell does not overcome the basic deficiencies of Kawakubo and Azuma, and certainly does not lend any credence to the proposed combination of these references. Therefore, the claims are believed patentable over the cited prior art for the reasons previously advanced.

Regarding the first full paragraph on page 5 under "Claim Rejections - 35 USC § 103" of the above-identified Office Action, rejecting claims 19, 20, and 22 as being unpatentable over Kawakubo in view of Azuma and further in view of Kirlin et al. (U.S. 5,976,928) (hereinafter "Kirlin") under 35 U.S.C. § 103(a), the Examiner states that the motivation for modifying Kawakubo and Azuma by Kirlin is "to use the slurry taught by Kirlin et al in order to effectively remove the metal and dielectric materials that are commonly used in capacitor structures...." It is respectfully submitted that

this statement is incorrect and is no more than wishful thinking on the part of the Examiner based on hindsight reconstruction of the prior art to arrive at the claimed invention.

The foregoing discussions of Kawakubo and Azuma are equally applicable in the instant rejection of claims 19, 20, and 22, which depend directly or indirectly on independent claim 1.

Kirlin does not make up for the deficiencies of Kawakubo and Azuma, individually or in the combination of these references. Therefore, claims 19, 20, and 22 are believed patentable over the prior art for the same reasons as previously advanced.

The Honorable Board is therefore respectfully urged to reverse the final rejection of the Supervisory Primary Examiner.

Respectfully submitted,

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Appendix - Appealed Claims:

1. A method of producing a structured layer, which comprises the following steps:

providing a prestructured substrate;

applying to the prestructured substrate a precious metal and a donor material containing an additive which is not a precious metal in two or more layers;

subjecting the layers to heat treatment at a temperature of between approximately 400°C and approximately 800°C, such that the additive diffuses into the precious metal and an alloy layer is produced; and

polishing the alloy layer by chemical and mechanical means.

2. The method according to claim 1, wherein the donor material essentially comprises only the additive.

3. The method according to claim 1, which comprises applying the donor material to the substrate before the precious metal.

7. The method according to claim 1, wherein the thickness of the donor material is selected such that during heat treatment

the donor material essentially diffuses completely into the precious metal.

11. The method according to claim 1, wherein the precious metal is an element from Group 8b of the Periodic Table of the Elements and/or is Au.

12. The method according to claim 11, wherein the precious metal is from Group 8b of the Periodic Table of the Elements and/or is Ir.

13. The method according to claim 1, wherein the additive is Ti, TiO_x, Ta, W, Bi, Ru and/or Pd.

15. The method according to claim 1, wherein the donor material is Ti, TiO_x, TiN, Ta, TaN, W, WN, Bi, BiO_x, IrO_x, $IrHfO_x$, RuO_x and/or PdO_x.

17. The method according to claim 1, wherein the alloy layer produced contains between approximately 5 and approximately 30 atom % of the donor material.

19. The method according to claim 1, wherein a slurry containing water, abrasive particles and at least one oxidant is used for the chemical mechanical polishing.

20. The method according to claim 19, wherein Al_2O_3 particles or SiO_2 particles are used as the abrasive particles.

21. The method according to claim 19, wherein the abrasive particles have a size of approximately 50 to 300 nm.

22. The method according to claim 19, wherein H_2O_2 is used as the at least one oxidant.

23. The method according to claim 19, wherein the slurry has at least one stabilizer.